TFT LCD Specification

MODEL NO.: PQ 3Qi-01

1. GENERAL DESCRIPTION

1.1 OVERVIEW

PQ 3Qi-01 is a 10.1" TFT Liquid Crystal Display module with LED backlight unit and 40 pin LVDS interface. This module supports 1024 x RGB x 600 Wide-SVGA (WSVGA) mode and can display 262,144 colors. This module also supports two low power modes: a transflective mode with lower color and a reflective black and white (64 grayscales) mode. In reflective mode the screens shows higher resolution at 3072 x 600 pixels, in transflective mode the color resolution is 1024 x RGB x 600, while the black/white/grey resolution is 3072 x 600. The converter module for the LED backlight is built in.

1.2 FEATURES

- Transmissive, Transflective, and Reflective display modes
- Sunlight readable
- Low power (~5X power reduction compared to standard 10" LCD)
  total power including TCON, DC-DC, Driver ICs, and LCD = ~0.4W with backlight off
- 3X luminance resolution (in black/white/grey) in transflective and reflective modes.
  This increased resolution can be effectively used with sub-pixel rendering and with MPG, JPG, and TV compression schemes which use 3-4X higher luminance channel resolution compared with chrominance channel resolution. This display can support such an encoding scheme with 3X higher resolution in luminance than in chrominance (e.g. color).

1.3 APPLICATION

- TFT LCD notebooks, netbooks, tablets, and e-reading devices.

1.4 GENERAL SPECIFICATI0NS

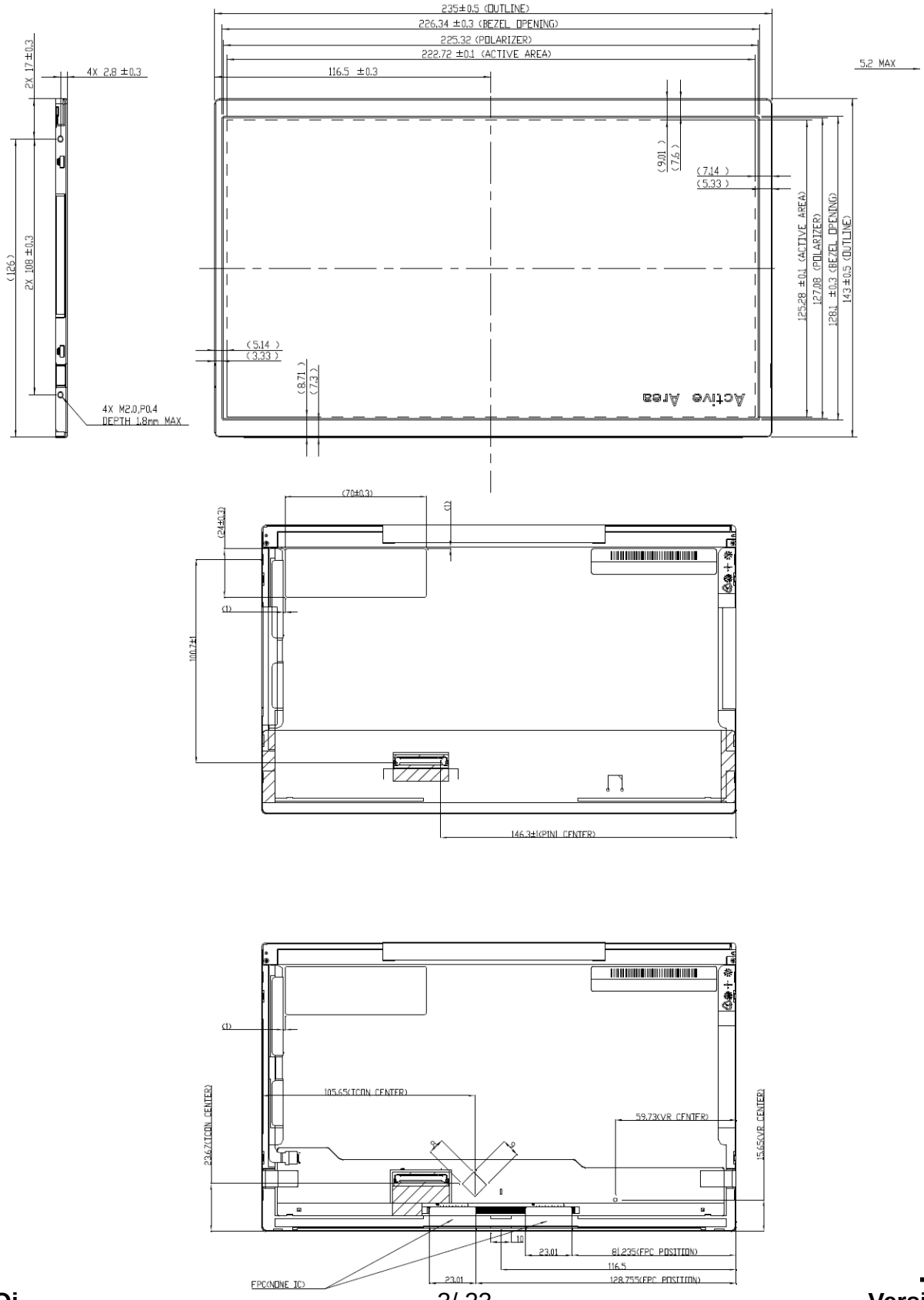
Item	Specification	Unit	Note
Active Area	222.72 (H) x 125.28 (V) (10.06” diagonal)	mm	(1)
Bezel Opening Area	226.34 (H) x 128.1 (V)	mm	
Pixel Number	1024 x R.G.B. x 600	pixel	(2)
Pixel Pitch	0.2175 (H) x 0.2088 (V)	mm	-
Pixel Arrangement	RGB vertical stripe + 3 reflective subpixels	-	-
Display Colors	262,144	color	-
Display Operating Modes	Transmissive, transflective, reflective	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	234.5	235.0	235.5	mm	(1)
	Vertical(V)	142.5	143.0	143.5	mm	
	Thickness(T)	-	4.9	5.2	mm	
Weight		-	185	195	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Each pixel is composed of 3 transmissive subpixels (RGB) and 3 reflective subpixels (grayscale).



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

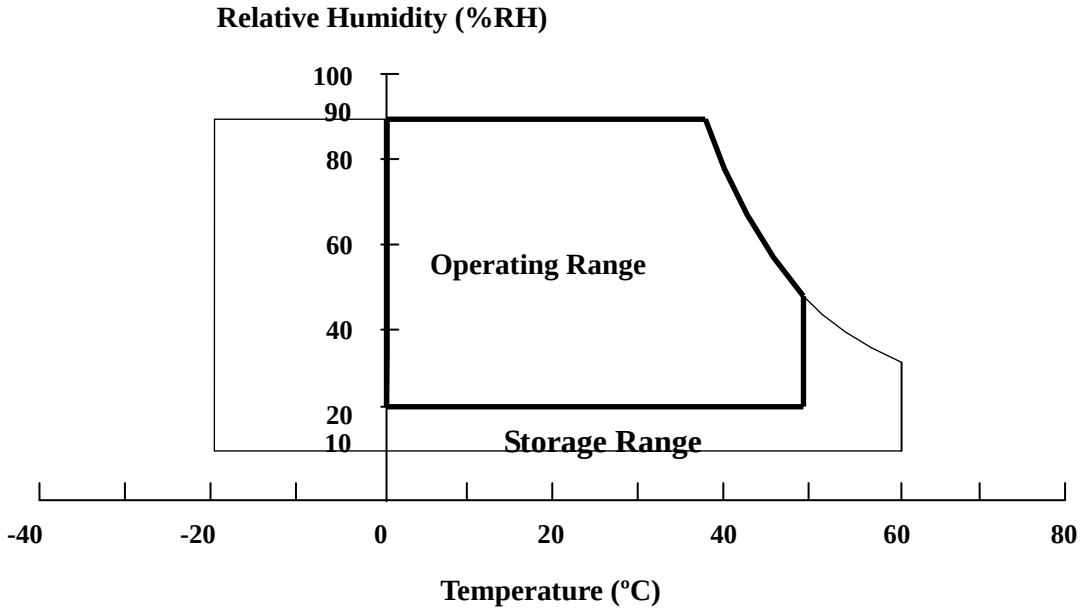
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface area should be 0 ºC min. and 60 ºC max.

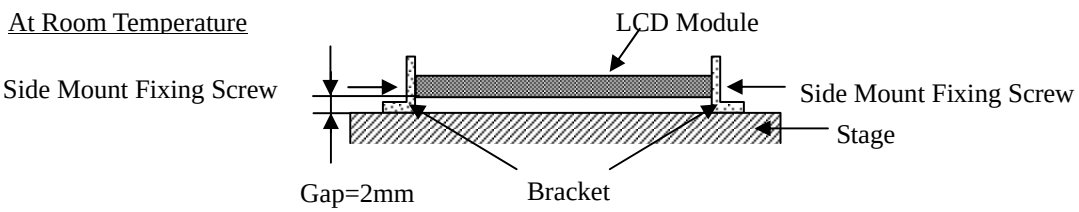


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave.

Note (4) 10~500 Hz, 30 min/cycle, 1 cycle for X, Y, Z-axis.

Note (5) When testing vibration and shock, the fixture holding the module has to be hard and rigid enough so that the module is not twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	V_{CC}+0.3	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

2.2.2 BACKLIGHT UNIT

Item	Value		Unit	Note
	Min	Max.		
LED Converter Input Voltage	-0.3	25	V	(1)
Converter control signal input voltage (LED_PWM, LED_EN)	-0.3	5.5	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

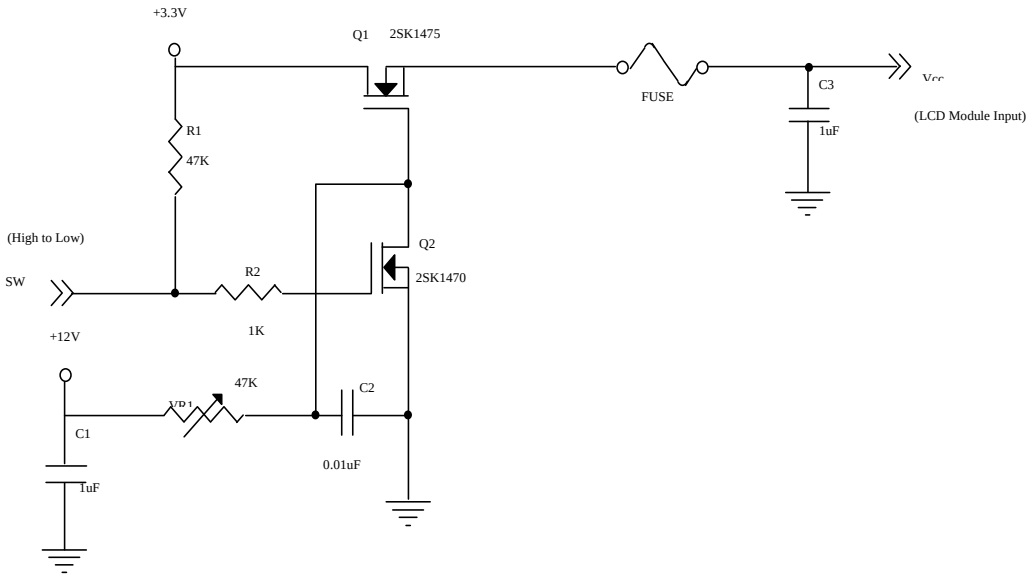
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	50		mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.0	A	(2)
Power Supply Current	White	Icc	179	203	228	mA	(3)a
	Black		135	153	171	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(5) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100	-	600	mV	(5)
Terminating Resistor		R_T	-	100	-	Ohm	-

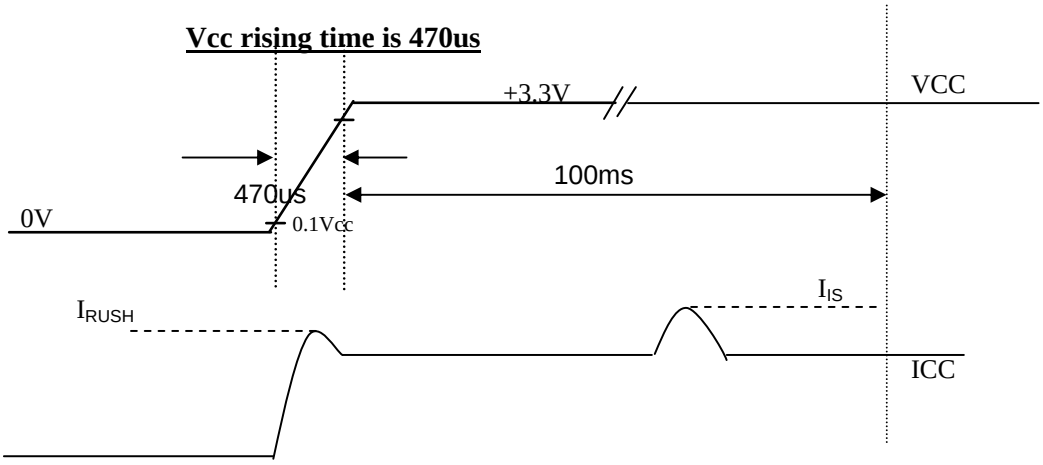
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown in the following figure. Test pattern: black.





Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, DC and f_v = 60 Hz, with a power dissipation check pattern (below) displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power is the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

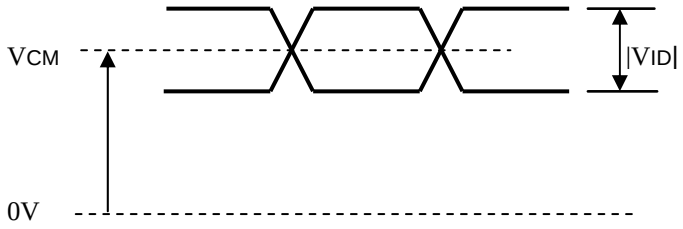
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

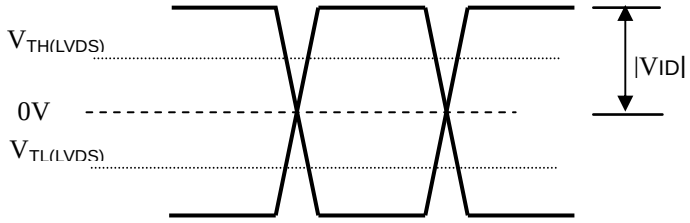
Note that luminance for this measurement is entirely from the backlight. In typical usage with some ambient light, the reflective component of the image allows lower power consumption at 60 nits.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential



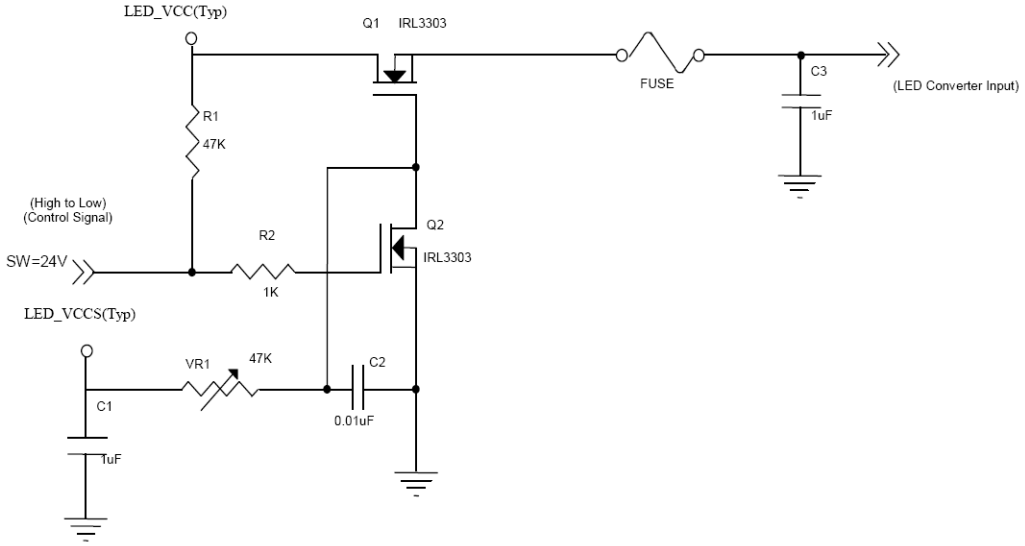
3.2. LED BACKLIGHT SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	4.5	18.7	21.0	V	
Converter Rush Current		$ILED_{RUSH}$			1.5	A	(1)
Converter Initial Stage Current		$ILED_{IS}$			1.5	A	(1)
EN Control Level	Backlight on	LED_EN	2.3	-	5.5	V	
	Backlight off		0	-	0.8	V	
PWM Control Level	PWM High Level	PWM	2.3	-	5.5	V	
	PWM Low Level		0	-	0.8	V	
PWM Control Duty Ratio			10	-	100	%	(2)
PWM Control Ripple Voltage		V_{PWM_pp}		-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	2000	Hz	(3)
LED Supply Current	LED_VCCS=Min	ILED	388	452	525	mA	(4)
	LED_VCCS=Typ		91	109	129	mA	(4)
	LED_VCCS=Max		83	97	113	mA	(4)
Power Consumption Backlight at highest brightness settling)		P_{OTM}		2.04		W	(5)(6) Duty 100%
Power Consumption (Reflective Mode Backlight Off		P_{ORF}		0		W	(5)
LED Life Time		L_{BL}	15000	-		Hrs	(7)

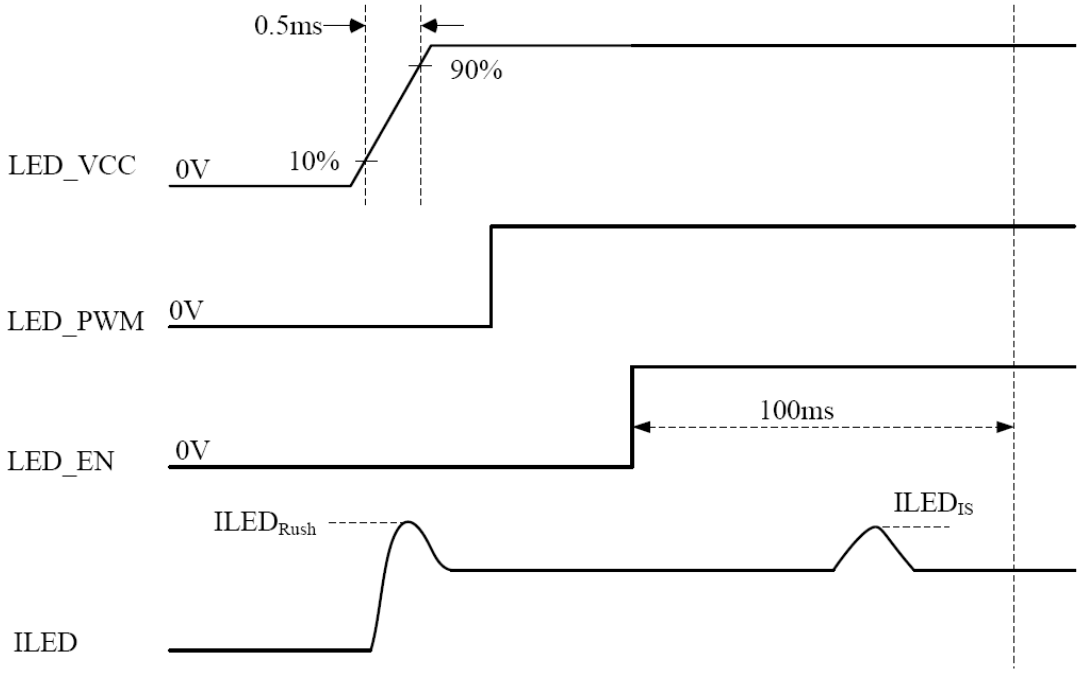
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCC is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCC = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1 kHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer ($N \geq 3$)

f : Frame rate

Note (4) The specified LED power supply current is under the conditions at "LED_VCC = Min., Typ., Max.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (5) In Transmissive mode, power is given for typical voltage at 100% duty cycle. Dimming the backlight (reducing duty cycle) will reduce power in Transmissive mode. In Transflective mode, duty cycle is typically lower than Transmissive mode. Lower or higher PWM duty cycle will result in lower

or higher power consumption, respectively. In Transflective mode, panel brightness depends on backlight power and reflected ambient light.

In reflective mode, the backlight is turned off. Light bar power consumption is zero.

Note (6) $P_O = I_O \times V_O$

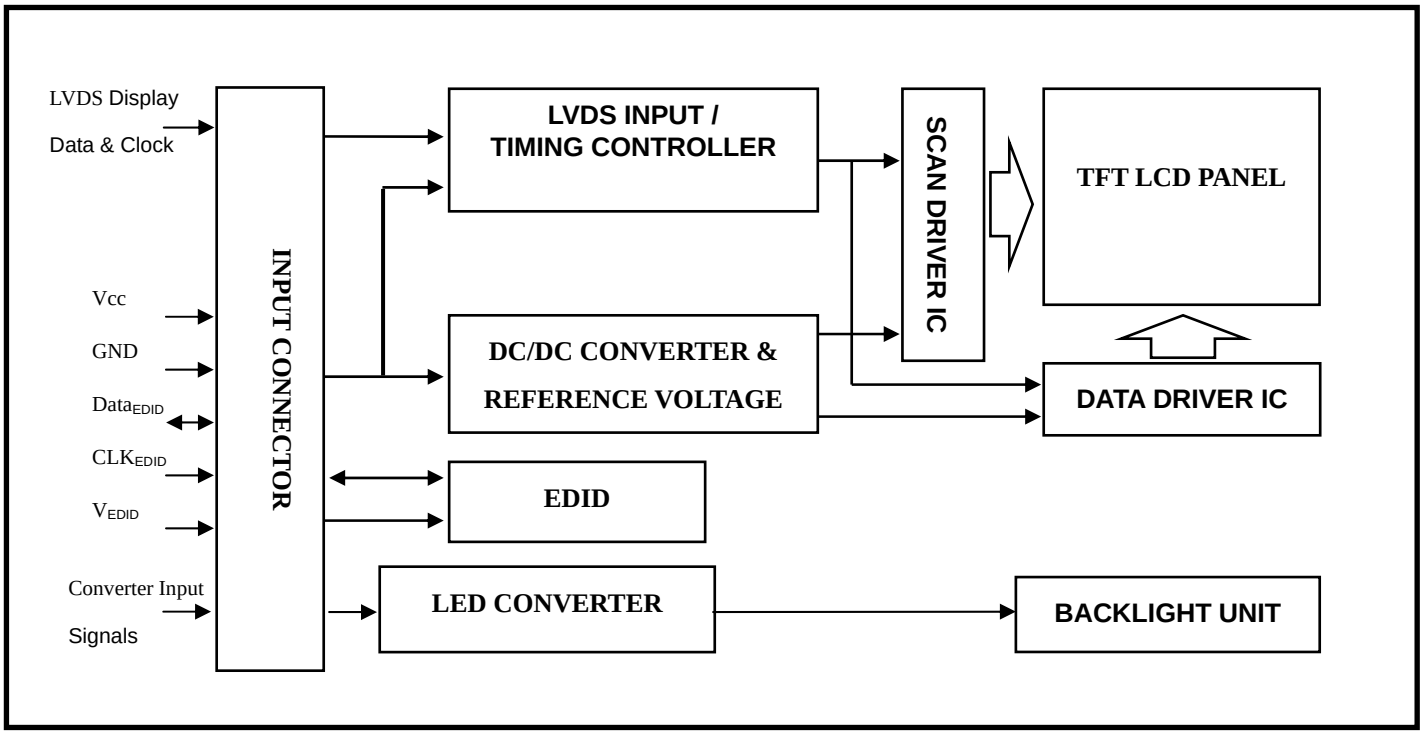
Note (7) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I = 17 mA (Per EA) until the brightness becomes ≦ 50% of its original value.

3.3 PANEL POWER CONSUMPTION

	Typical	Notes
Panel Power Consumption (for backlight unit see table 3.2)	0.43 W	ANSI checkerboard pattern, 30 fps; includes LCD, TCON, Drivers, TFT and DC-DC
Total Panel Power Consumption (for backlight unit see table 3.2)	0.58 W	ANSI checkerboard pattern, 60 fps; includes LCD, TCON, Drivers, TFT and DC-DC

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

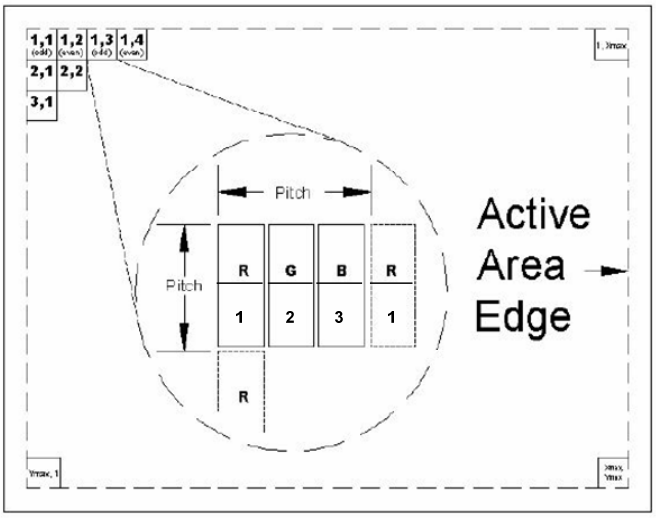
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	NC	No Connection (Reserve)		
2	VDD	Power Supply		
3	VDD	Power Supply		
4	VEDID	EDID power supply		Can be connected to VDD
5	NC	No Connection (Reserved for test)		
6	CLKEDID	DDC clock		
7	DATAEDID	DDC data		
8	Rxin0-	LVDS differential data input	Negative	R0-R5, G0
9	Rxin0+	LVDS differential data input	Positive	
10	VSS	Ground		
11	Rxin1-	LVDS differential data input	Negative	G1~G5, B0, B1
12	Rxin1+	LVDS differential data input	Positive	
13	VSS	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2-B5,HS,VS, DE
15	Rxin2+	LVDS Differential Data Input	Positive	
16	VSS	Ground		
17	RxCLK-	LVDS differential clock input		
18	RxCLK+	LVDS differential clock input		
19	VSS	Ground		
20	NC	No Connection (Reserve)		
21	NC	No Connection (Reserve)		
22	VSS	Ground		
23	NC	No Connection (Reserve)		
24	NC	No Connection (Reserve)		
25	VSS	Ground		
26	NC	No Connection (Reserve)		
27	NC	No Connection (Reserve)		
28	VSS	Ground		
29	NC	No Connection (Reserve)		
30	NC	No Connection (Reserve)		
31	VSS	LED Ground		
32	VSS	LED Ground		
33	VSS	LED Ground		
34	NC	No Connection (Reserve)		
35	PWM	LED BLU Brightness Control		
36	LED_EN	LED Converter Enable		
37	NC	No Connection (Reserve)		
38	VLED	LED Converter Input Power		
39	VLED	LED Converter Input Power		
40	VLED	LED Converter Input Power		

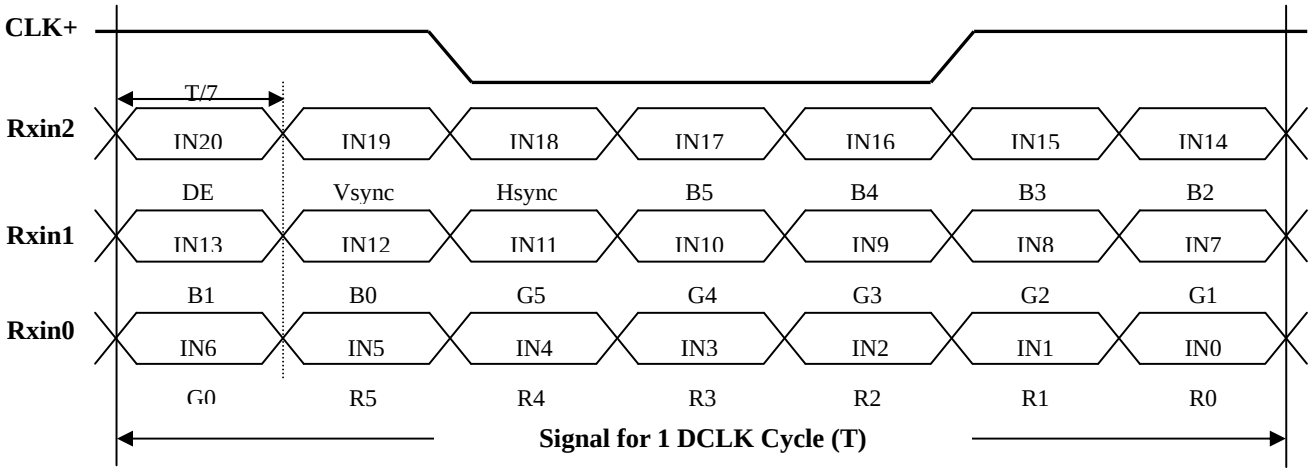
Note (1) Connector Part No.: IPEX-20455-040E-12 or equivalent

Note (2) User's connector Part No: IPEX-20453-040T-01 or equivalent

Note (3) The first pixel is odd as shown in the following figure.



5.2 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards. These values are preliminary.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“PQI”)	42	01000010
9	9	EISA ID manufacturer name (Compressed ASCII)	29	00101001
10	0A	ID product code (N101L8-L01)	08	00001000
11	0B	ID product code (hex LSB first; N101L8-L01)	10	00010000
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	28	00101000
17	11	Year of manufacture (fixed year code)	13	00010011
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Max H image size (“22.272cm”)	16	00010110
22	16	Max V image size (“12.528cm”)	0C	00001100
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“RGB Color”)	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	A3	10100011
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.549	8C	10001100
28	1C	Ry=0.342	57	01010111
29	1D	Gx=0.324	53	01010011
30	1E	Gy=0.550	8C	10001100
31	1F	Bx=0.158	28	00101000
32	20	By=0.161	29	00101001
33	21	Wx=0.313	50	01010000
34	22	Wy=0.341	57	01010111
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 2 40Hz Timing Pixel clock ("29.31MHz", According to VESA CVT Rev1.1)	2D	00101101
55	37	# 2 40Hz Timing Pixel clock (hex LSB first)	11	00010001
56	38	# 2 40Hz Timing H active (“1024”)	00	00000000
57	39	# 2 40Hz Timing H blank (“160”)	A0	10100000
58	3A	# 2 40Hz Timing H active : H blank (“1024 : 160”)	40	01000000
59	3B	# 2 40Hz Timing V active (”600”)	58	01011000
60	3C	# 2 40Hz Timing V blank (”19”)	13	00010011
61	3D	# 2 40Hz Timing V active : V blank (”600 :19”)	20	00100000
62	3E	# 2 40Hz Timing H sync offset (”48”)	30	00110000
63	3F	# 2 40Hz Timing H sync pulse width ("32”)	20	00100000
64	40	# 2 40Hz Timing V sync offset : V sync pulse width (”3 : 10”)	3A	00111010
65	41	# 2 40Hz Timing H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 10”)	00	00000000
66	42	# 2 40Hz Timing H image size (”222 mm”)	DE	11011110
67	43	# 2 40Hz Timing V image size (”125 mm”)	7D	01111101
68	44	# 2 40Hz Timing H image size : V image size (”222 : 125”)	00	00000000
69	45	# 2 40Hz Timing H boarder (”0”)	00	00000000
70	46	# 2 40Hz Timing V boarder (”0”)	00	00000000
71	47	# 2 40Hz Timing Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	18	00011000
72	48	Detailed timing description # 1 Pixel clock (“43.97MHz”, According to VESA CVT Rev1.1)	74	01110100
73	49	# 1 Pixel clock (hex LSB first)	0B	00001011
74	4A	# 1 H active (“1024”)	00	00000000
75	4B	# 1 H blank (“160”)	A0	10100000
76	4C	# 1 H active : H blank (“1024 : 160”)	40	01000000
77	4D	# 1 V active (”600”)	58	01011000
78	4E	# 1 V blank (”19”)	13	00010011

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
79	4F	# 1 V active : V blank (”600 :19”)	20	00100000
80	50	# 1 H sync offset (”48”)	30	00110000
81	51	# 1 H sync pulse width ("32”)	20	00100000
82	52	# 1 V sync offset : V sync pulse width (”3 : 10”)	3A	00111010
83	53	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 10”)	00	00000000
84	54	# 1 H image size (”222 mm”)	DE	11011110
85	55	# 1 V image size (”125 mm”)	7D	01111101
86	56	# 1 H image size : V image size (”222 : 125”)	00	00000000
87	57	# 1 H boarder (”0”)	00	00000000
88	58	# 1 V boarder (”0”)	00	00000000
89	59	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
90	5A	Detailed timing description # 3 30Hz Timing Pixel clock ("21.99MHz”, According to VESA CVT Rev1.1)	97	10010111
91	5B	# 3 30Hz Timing Pixel clock (hex LSB first)	08	00001000
92	5C	# 3 30Hz Timing H active (“1024”)	00	00000000
93	5D	# 3 30Hz Timing H blank (“160”)	A0	10100000
94	5E	# 3 30Hz Timing H active : H blank (“1024 : 160”)	40	01000000
95	5F	# 3 30Hz Timing V active (”600”)	58	01011000
96	60	# 3 30Hz Timing V blank (”19”)	13	00010011
97	61	# 3 30Hz Timing V active : V blank (”600 :19”)	20	00100000
98	62	# 3 30Hz Timing H sync offset (”48”)	30	00110000
99	63	# 3 30Hz Timing H sync pulse width ("32”)	20	00100000
100	64	# 3 30Hz Timing V sync offset : V sync pulse width (”3 : 10”)	3A	00111010
101	65	# 3 30Hz Timing H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 10”)	00	00000000
102	66	# 3 30Hz Timing H image size (”222 mm”)	DE	11011110
103	67	# 3 30Hz Timing V image size (”125 mm”)	7D	01111101
104	68	# 3 30Hz Timing H image size : V image size (”222 : 125”)	00	00000000
105	69	# 3 30Hz Timing H boarder (”0”)	00	00000000
106	6A	# 3 30Hz Timing V boarder (”0”)	00	00000000
107	6B	# 3 30Hz Timing Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	18	00011000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name“PQ3Qi-01”, ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name (“P”)	50	01010000
114	72	# 4 2nd character of name (“Q”)	51	01010001
115	73	# 4 3rd character of name (“3”)	33	00110011
116	74	# 4 4th character of name (“Q”)	51	01010001
117	75	# 4 5th character of name (“i”)	69	01101001
118	76	# 4 6th character of name (“-")	2D	00101101

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
119	77	# 4 7th character of name (“0”)	30	00110000
120	78	# 4 8th character of name (“1”)	31	00110001
121	79	# 4 New line character indicates end of ASCII string	0A	00001010
122	7A	# 4 Padding with “Blank” character	20	00100000
123	7B	# 4 Padding with “Blank” character	20	00100000
124	7C	# 4 Padding with “Blank” character	20	00100000
125	7D	# 4 Padding with “Blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	E5	11100101

6. INTERFACE TIMING

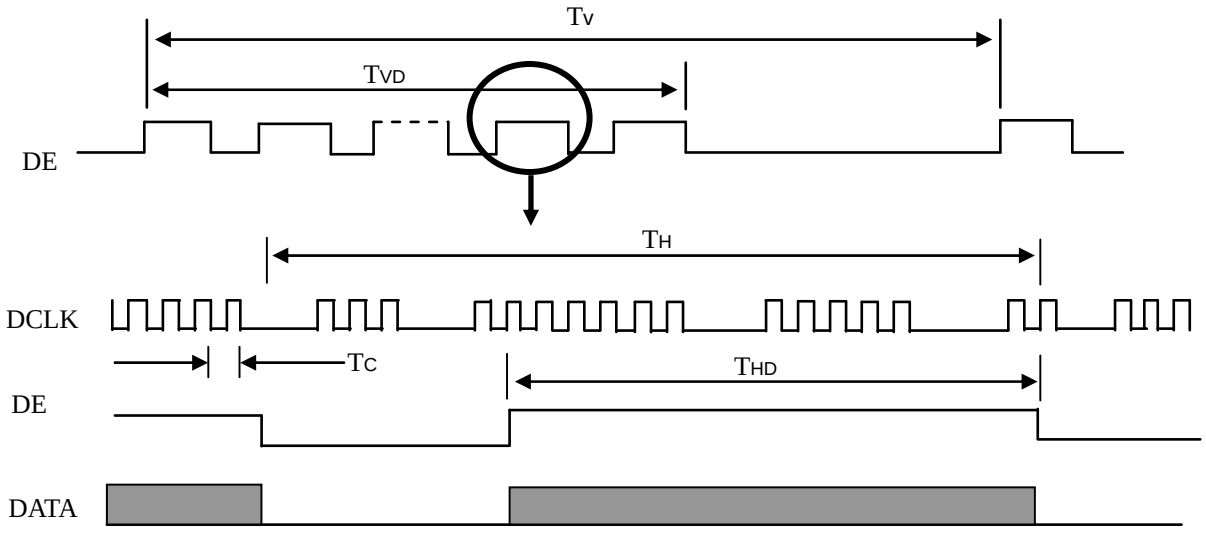
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram**.**

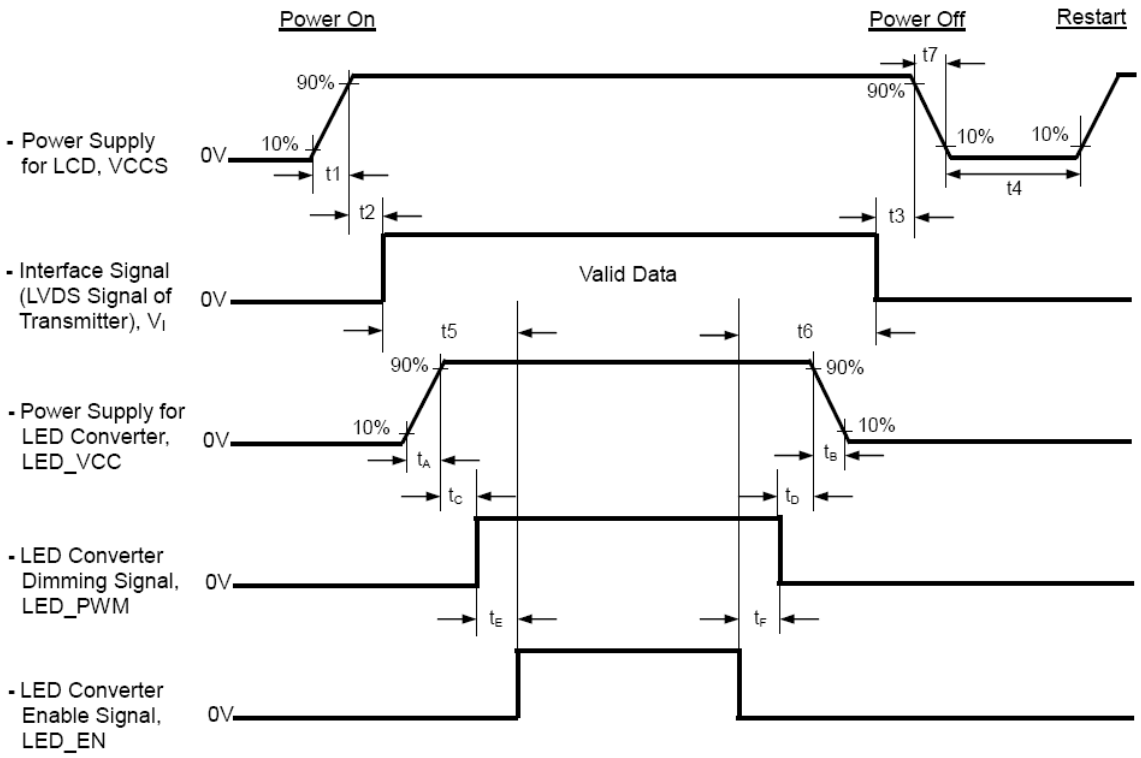
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	21.74	43.97	46.15	MHz	-
DE	Vertical Total Time	TV	602	619	624	TH	-
	Vertical Active Display Period	TVD	600	600	600	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	19	TV-TVD	TH	-
	Horizontal Total Time	TH	1104	1184	1240	Tc	-
	Horizontal Active Display Period	THD	1024	1024	1024	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Note (1) Because this module is operated in DE only mode, Hsync and Vsync are ignored.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5≦ t1 ≦ 10 ms

0 ≦ t2 ≦ 50 ms

0 ≦ t3 ≦ 50 ms

t4 ≧ 500 ms

t5 ≧ 200 ms

t6 ≧ 200 ms

0.5≦ t7 ≦ 10 ms

0.5≦ t_A ≦ 10 ms

0 < t_B ≦ 10 ms

t_C ≧ 10 ms

t_D ≧ 10 ms

t_E ≧ 10 ms

t_F ≧ 10 ms

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be

damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, the Vcc falling time should follow 50us ≦ t7 ≦10 ms.

6.3 DISPLAY MODE CONTROL

The display panel supports 3 modes: purely reflective, purely transmissive, and transflective. The mode is set by the ambient light intensity and backlight intensity. The following truth table shows how different modes are selected.

Condition			Description	
Ambient Light	Backlight		Mode	Notes
Non-dark	Off		Reflective	Backlight off, reflective subpixels active, grayscale image, minimum power mode.
Dark	On		Transmissive	Conventional display mode. Backlight on, reflective subpixels black due to absence of ambient light, saturated colors.
Non-dark	On		Transflective	Backlight on, reflective subpixels reflecting ambient light, colors desaturated, power reduced if backlight dimmed.

7. PRECAUTIONS

7.1 SYSTEM MATCHING PRECAUTIONS

(1) Refer to the drawing.

(2) To avoid wireless noise interference, please keep the antenna away from LCD control board.

7.2 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity; it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

7.3 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slower.

7.4 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) Do not disassemble the module or insert anything into the Backlight unit.

(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.